REMARKS

This is intended as a full and complete response to the Second Office Action dated November 17, 2006 (hereinafter "the Office Action") having a shortened statutory period for response set to expire on February 17, 2006.

Claims 1-27 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,487,648 ("Hassoun") in view of U.S. Patent No. 5,625,580 ("Read"), and further in view of U.S. Patent No. 5,920,600 ("Yamaoka"). With this rejection, Applicants respectfully disagree, at least for the reasons set forth below.

It is now well established that the Patent Office bears the burden of establishing a *prima facie* case to maintain a rejection for obviousness. Failure to make such a *prima facie* showing by the Patent Office is to result in a withdrawing of the rejection. Applicants' position is that the Patent Office has failed to make such a *prima facie* showing, and thus the rejection of Claims 1-27 under 35 U.S.C. § 103(a) should be withdrawn.

The MPEP states what the Patent Office considers to be a "*prima facie* case" of obviousness at Section 706.02(j). Taking *arguendo* the Patent Office criteria of a "*prima facie* case" of obviousness as the standard, it will become apparent that the instant rejection for obviousness fails to meet such criteria and, accordingly, that the rejection of Claims 1-27 for obviousness is improper and should be withdrawn.

According to the Patent Office, the first element of a *prima facie* case for obviousness is that there must be some suggestion or motivation to modify a reference or combine the teachings of the references. This suggestion must come from either of the references or be knowledge generally available to one of ordinary skill in the art.

In the Office Action, it is asserted, incorrectly, that Hassoun, Read, and Yamaoka are analogous. Clearly these references are not analogous. Hassoum is for an SDRAM controller for implementation in a PLD. Read is for a hardware modeling system. Yamaoka is for bit phase synchronization for high-speed data transmission systems. These references are in three separate fields of endeavor. Nor are these disparate references directed to the same problem. Hassoun is directed at reducing

lead time for development of an SDRAM controller. Read is directed at integrating a hardware modeling system to various simulator platforms, support for ASICs, prototype verification of ASICs, and direct timing measurement of HME output delays. Yamaoka is directed at phase synchronizing incoming transmitted data to a clock of a receiver. Applicants thus respectfully submit that the only possible basis for combining these references as used in the Office Action is an improper one, namely improper hindsight reconstruction in the light of Applicants' claimed invention.

In the Office Action, it is asserted, incorrectly, that combination of these three references is motivated by "...the advantage of achieving high performance easily and at low cost ... reliability and lower cost manufacturing system ... and further ...an improvement [sic] modeling system ...." In other words, the Office Action offers only general motives for combining these references. Assuming *arguendo* that these objectives may be met by the combination proffered in the Office Action, these general motives do not provide a legally sufficient suggestion or motivation for such combination. The Federal Circuit has said that "[a] general relationship between fields of the prior art patents to be combined is insufficient to establish the suggestion or motivation." (*Interactive Techs. v. Pittway Corp.*, Civ. App. No. 98-1464, slip op. at 13 (Fed. Cir. June 1, 1999) (*unpublished*), *cert. denied*, 528 U.S. 1046 (1999).)

In the instant rejection, nothing in the Office Action indicates that there is any suggestion in either of the references for this combination other than the general motives cited as taken from Yamaoka and Read. Thus, the combination cannot rest upon any suggestion in either of the references. Moreover, it is Applicants' position that the above-quoted statements regarding these references provide no reasonable basis for the assertion that one of ordinary skill in the art would be led to combine these three particular references out of all the references potentially available.

According to the Patent Office, the second element of a *prima facie* case for obviousness is that there must be a reasonable expectation of success. As an initial matter, the Office Action does not even address the issue of a reasonable expectation of success. Given that the burden rests with the Patent Office to demonstrate obviousness, this failure to present evidence for this element of the *prima facie* case suggests that the rejection on the basis of obviousness should be withdrawn.

Applicants are placed in the position of responding to an argument regarding a reasonable expectation of success that has not been made by the Office Action. In order to ascertain whether there would be such a reasonable expectation of success, there must be some understanding of how the primary reference of Hassoun is to be modified by the secondary references of Read and Yamaoka to arrive at the claimed invention. Presently, there is no indication in the Office Action of how the teachings of Hassoun are to be reengineered in view of the teachings of Read and Yamaoka to arrive at the claimed invention. Again, as both Hassoun and Read are silent as to detecting clock stabilization, there is no basis to provide any indication of how the references may be modified to detect clock stabilization. Furthermore, as indicated below, Yamaoka too is silent as to detecting clock stabilization as claimed.

According to the Patent Office, the third element of a *prima facie* case for obviousness is that the cited prior art references must teach or suggest all the claim limitations.

Assuming *arguendo* that modification of Hassoun by Read and Yamaoka is proper, which it is not, Applicants agree with the statements in the Office Action that Hassoun as modified by Read clearly does not teach detecting clock stabilization and masking of an output, as claimed. Applicants note from a reading of the Office Action in comparison with the prior Official Action that the several inconsistencies regarding Hassoun and Read arise from using text from the prior Official Action without modification. Accordingly, in view of the prosecutorial history, Applicants believe the current position of the Patent Office is that Hassoun as modified by Read clearly does not teach detecting clock stabilization and masking of an output, as claimed.

Applicants renew their previously made remarks of record regarding Hassoun and Read, and now address the newly added text forming the rejection in the current Office Action. At the outset, Applicants disagree with the characterization of Yamaoka in the Office Action.

Applicants respectfully submit that what Yamaoka actually discloses is a phase selector (Yamaoka at FIG. 28) that detects a stable phase timing based on a best phase fit of multiphase (e.g., multiphase clocks 2011-1 through 2011-n) synchronizing to a pattern in a preamble of burst cell data. (Yamaoka, at col. 19, line 3, to col. 21,

line 5.) Responsive to establishing synchronization with such a pattern, the data 2017-1 through 2017-3 are output from the phase selector, where data 2017-2 is of the most stable phase, and data 2017-1 and 2017-3 are next to data 2017-2. (*Id.*) Additionally, the phase selector is configured to prevent a selection controller from going into a tracking type synchronization mode until after synchronization has been established by selection of a best phase fit multiphase clock. (*Id.*)

However, stability as to synchronization of a clock with a data timing pattern in Yamaoka is not masking an output signal until the output clock signal is sufficiently stabilized as indicated by a control signal for hardware simulation, as claimed in the pending independent claims, namely Claims 1, 8, 11, 12, 13, 14, 24, and 27. Furthermore, controlling a transition between a selection type synchronization mode and a tracking type synchronization mode as in Yamaoka is not what is being claimed. Additionally, Yamaoka does not disclose determining stability prior to application of a master clock for selection of a multiphase clock. (*E.g.*, Yamaoka at col. 19, line 67, to col. 20, line 10, makes no mention of first stabilizing a master clock before application thereof.)

Accordingly, it is respectfully submitted that Claims 1, 8, 11, 12, 13, 14, 24, and 27 are in condition for allowance and such allowance is respectfully requested. Furthermore, Claims 2-7, 9-10, 15-23, and 25-26, which either directly or indirectly depend upon an allowable base claim, are likewise allowable.

Additionally, it is respectfully submitted that the rejection of Claims 1-27 under 35 U.S.C. § 103(a) as being obvious over Hassoun in view of Read and Yamaoka is improper and should be withdrawn for any of the several reasons provided above, and it is respectfully requested that the Application be passed to issuance.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on February 6, 2007.

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